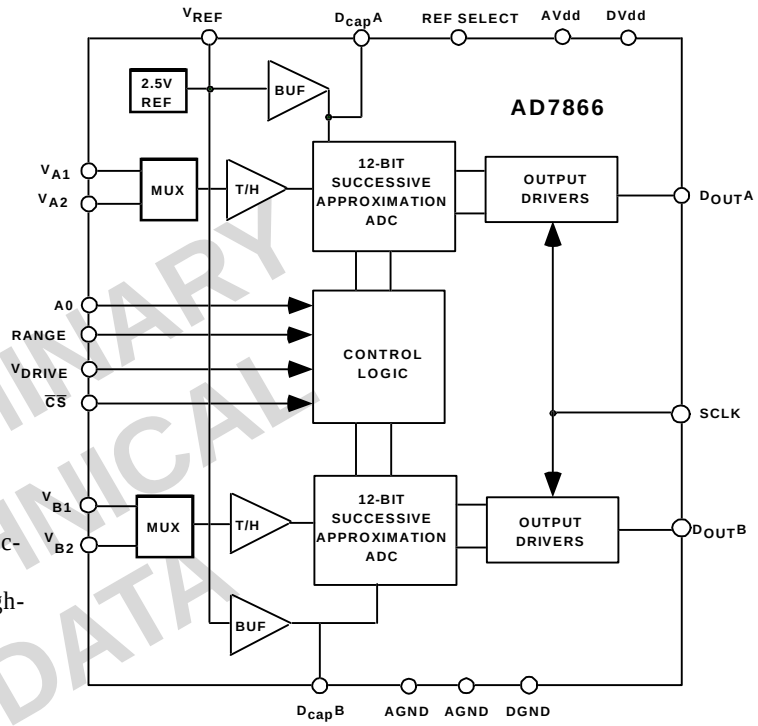
Dual 1MSPS, 12-Bit, 2-Channel SAR ADC with Serial Interface

Preliminary Technical Data — AD7866

FEATURES

Dual 12-bit 2-channel ADC
Fast Throughput Rate: 1MSPS
Specified for V_{DD} of 2.7 V to 5.25 V
Low Power:
9mW Max at 1MSPS with 3V Supplies
30mW Max at 1MSPS with 5V Supplies
Wide Input Bandwidth:
70dB SNR at 500kHz Input Frequency
Onboard Reference 2.5V
Flexible Power/Throughput Rate Management
Simultaneous Conversion/Read
No Pipeline Delays
High Speed Serial Interface
Shut Down Mode: 1µA typ.
20-Pin TSSOP Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7866 is a dual 12-bit high speed, low power, successive-approximation ADC. The part operates from a single 2.7 V to 5.25 V power supply and features throughput rates up to 1MSPS. Both devices contain two low-noise, wide bandwidth track/hold amplifiers which can handle input frequencies in excess of 1MHz.

The conversion process and data acquisition are controlled using standard control inputs allowing easy interfacing to microprocessors or DSPs. The input signal is sampled on the falling edge of $\overline{CS}$ and conversion is also initiated at this point. The conversion time is determined by the SCLK.There are no pipelined delays associated with the part.

The AD7866 uses advanced design techniques to achieve very low power dissipation at high throughput rates. With 3V supplies and 1MSPS throughput rate, the part consumes approximately 3mA. With 5V supplies and 1MSPS, the current consumption is approximately 6mA. The part also offers flexible power/throughput rate management when operating in sleep mode.

The analog input range for the part can be selected to be a 0 to V_{REF} input or a 0 to 2* V_{REF} with either straight binary or 2s complement output coding. The AD7866 has an on-chip +2.5V reference which can be overdriven if an external reference is preferred. Each ADC can be supplied with an individual external reference.

The AD7866 is available in a 20-pin thin shrink small outline (TSSOP) package.

PRODUCT HIGHLIGHTS

1. The AD7866 features two complete ADC func tions allowing simultaneous sampling and conversion of two channels. Each ADC has a 2-channel input multi plexer. The conversion result of both channels is avail able simultaneously.
2. High Throughput with Low Power Consumption
   The AD7866 offers a 1MSPS throughput rate with 9mW power consumption when operating at 3V.
3. Flexible Power/Throughput Rate Management
   The conversion rate is determined by the serial clock allowing the power consumption to be reduced as the conversion time is reduced through a SCLK frequency increase . Power efficiency can be maximized at lower throughput rates if the part enters sleep during conver sions.
4. No Pipeline Delay.
   The part features two standard successive-approximation ADCs with accurate control of the sampling instant via a $\overline{CS}$ input and once off conversion control.

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AD7866–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, VREF = 2.5 V, f_{SCLK} = 20 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	Units	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Signal to Noise Ratio (SNR)[2]	71	dB min	f_{IN} =455KHz Sine Wave, f_S =1MSPS
Signal to Noise + Distortion (SINAD)[2]	70	dB min	f_{IN} =455KHz Sine Wave, f_S =1MSPS
Total Harmonic Distortion (THD)	–76	dB max	f_{IN} =455KHz Sine Wave, f_S = 1MSPS
Peak Harmonic or Spurious Noise (SFDR)	–76	dB max	f_{IN} =455KHz Sine Wave, f_S = 1MSPS
Intermodulation Distortion (IMD)			
Second Order Terms	-76	dB typ	
Third Order Terms	-76	dB typ	
Channel to Channel Isolation	-80	db typ	
SAMPLE AND HOLD			
Aperature Delay[3]	10	ns max	
Aperature Jitter[3]	50	ps typ	
Aperature Delay Matching[3]	50	ps max	
Full Power Bandwidth	20	MHz typ	
DC ACCURACY			
Resolution	12	Bits	
Integral Nonlinearity	±1.5	LSB max	
Differential Nonlinearity	±0.9	LSB max	Guaranteed No Missed Codes to 12 Bits.
Offset Error	±5	LSB max	
Offset Error Match	±5	LSB max	
Gain Error	±2	LSB max	
Gain Error Match	±2	LSB max	
ANALOG INPUT			
Input Voltage Ranges	0 to V_{REF}	Volts	RANGE pin tied low upon $\overline{CS}$ falling edge.
	0 to $2V_{REF}$	Volts	RANGE pin tied high upon $\overline{CS}$ falling edge.
dc Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REFERENCE INPUT/OUTPUT			
REF IN Input Voltage Range	2.5	V	+/-1% for Specified Performance
	2/3	Vmin/Vmax	REF SELECT pin tied high.
dc Leakage Current	±1	µA max	
Input Capacitance	20	pF typ	
REF OUT Output Voltage	2.45/2.55	Vmin/Vmax	
REF OUT Error @ 25c	tbd		
REF OUT Error (Tmin to Tmax)	tbd		
REF OUT Temperature Coefficient	50	ppm/C	
REF OUT Output Impedance	tbd		
LOGIC INPUTS			
Input High Voltage, V_{INH}	2.8	V min	V_{DRIVE} = 5V
	2.4	V min	V_{DRIVE} = 3V
Input Low Voltage, V_{INL}	0.4	V max	
Input Current, I_{IN}	±1	µA max	Typically 10 nA, V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]	10	pF max	
LOGIC OUTPUTS			
Output High Voltage, V_{OH}	V_{DRIVE} -0.2	V min	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} =200 µA
Floating-State Leakage Current	±10	µA max	V_{DD} = 2.7 V to 5.25 V
Floating-State Output Capacitance	10	pF max	
Output Coding	Straight(Natural) Binary		
	2s Complement		
CONVERSION RATE			
Conversion Time	16	SCLK cycles	800ns with SCLK = 20MHz
Track/Hold Acquisition Time	200	ns max	
Throughput Rate	1	MSPS max	Tconv + Tquiet

AD7866–SPECIFICATIONS[1]

(V_{DD} = +2.7 V to +5.25 V, VREF = 2.5 V, f_{SCLK} = 20 MHz unless otherwise noted; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	A Version[1]	Units	Test Conditions/Comments
POWER REQUIREMENTS			
V_{DD}	+2.7/+5.25	V min/max	
V_{DRIVE}	+2.7/+5.25	V min/max	
I_{DD}[4]			Digital I/Ps = 0V or DV_{DD}
Normal Mode(Static)	2.1	mA max	V_{DD} = 4.75V to 5.25V.
		mA max	V_{DD} = 2.7V to 3.6V.
Normal Mode(Operational)	6	mA max	V_{DD} = 4.75V to 5.25V. f_S=1MSPS
	3	mA max	V_{DD} = 2.7V to 3.3V. f_S=1MSPS
Partial Power-Down Mode	1.6	mA max	f_S=100kSPS, f_{SCLK} = 20MHz
Partial Power-Down Mode	TBD	µA max	(Static)
Full Power-Down Mode	1	µA max	SCLK on or off. Digital I/Ps = 0V or V_{DRIVE}
Power Dissipation[4]			
Normal Mode(Operational)	30	mW max	V_{DD} = 5V.
	9	mW max	V_{DD} = 3V
Partial Power-Down (Static)	TBD	uW max	V_{DD} = 5 V. SCLK on or off.
	TBD	µW max	V_{DD} = 3 V. SCLK on or off.
Full Power-Down (Static)	5	uW max	V_{DD} = 5 V. SCLK on or off.
	3	µW max	V_{DD} = 3 V. SCLK on or off.

NOTES
[1]Temperature ranges as follows: A, B Versions: –40°C to +85°C.
[2]SNR calculation includes distortion and noise components.
[3] Sample tested @ +25°C to ensure compliance.
[4] See POWER VERSUS THROUGHPUT RATE section.

Specifications subject to change without notice.

TIMING SPECIFICATIONS[1] (V_{DD} = +2.7 V to +5.25 V, VREF = 2.5 V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_{MIN}, T_{MAX} AD7866	Units	Description
f_{SCLK}[2]	10	kHz min	
	20	MHz max	
$t_{CONVERT}$	16*t_{SCLK}	ns max	t_{SCLK}= 1/f_{SCLK}
	800	ns max	f_{SCLK} = 20MHz
t_{quiet}	200	ns max	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_2	10	ns min	$\overline{CS}$ to SCLK Setup Time
t_3[3]	tbd	ns max	Delay from $\overline{CS}$ Until D_{OUT}A and D_{OUT}B 3-State Disabled
t_4[3]	10	ns max	Data Access Time After SCLK Falling Edge
t_5	0.4t_{SCLK}	ns min	SCLK Low Pulse Width
t_6	0.4t_{SCLK}	ns min	SCLK High Pulse Width
t_7	10	ns min	SCLK to Data Valid Hold Time
t_8[4]	25	ns max	SCLK Falling Edge to D_{OUT}A, D_{OUT}B, High Impedance
$t_{power-up}$	tbd	µs typ	Power up time from Full Power-down

NOTES

[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6 Volts. See Figure 2.

[2]Mark/Space ratio for the CLK input is 40/60 to 60/40.

[3]Measured with the load circuit of Figure 1 and defined as the time required for the output to cross 0.8 V or 2.0 V.

[4]t_8 is derived form the measured time taken by the data outputs to change 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics are the true bus relinquish times of the part and are independent of the bus loading.

Specifications subject to change without notice.

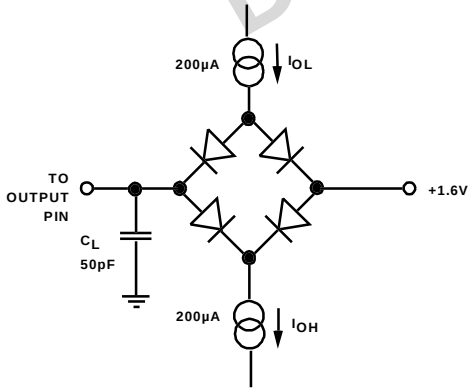


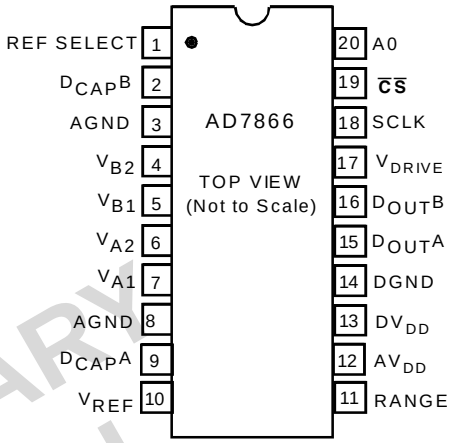
Figure 1. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS[1]

(T_A = +25°C unless otherwise noted)

AV_{DD} to AGND ..... -0.3V to +7V
DV_{DD} to DGND ..... -0.3V to +7V
V_{DRIVE} to DGND .....-0.3V to DV_{DD} +0.3V
AV_{DD} to DV_{DD} ..... -0.3V to +0.3V
AGND TO DGND ..... -0.3V to +0.3V
Analog Input Voltage to AGND .. -0.3V to AV_{DD}+0.3V
Digital Input Voltage to DGND ....-0.3V to DV_{DD}+0.3V
V_{REF} to AGND .....-0.3V to AV_{DD}+0.3V
Input Current to Any Pin Except Supplies[2] .....±10mA
Operating Temperature Range
Commercial (A Version) .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature ..... +150°C
TSSOP Package, Power Dissipation .....450 mW
q_{JA} Thermal Impedance.....115°C/W (TSSOP)
q_{JC} Thermal Impedance.....48°C/W (TSSOP)
Lead Temperature, Soldering
Vapor Phase (60 secs).....+215°C
Infared (15 secs).....+220°C

AD7866 PINCONFIGURATION TSSOP



NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Transient currents of up to 100 mA will not cause SCR latch up.

ORDERING GUIDE

Model	Range	Resolution (Bits)	Package Option[1]	
AD7866ARU	-40°C to +85°C	12	RU-20	
AD7866BRU	-40°C to +85°C	12	RU-20	
EVAL-AD7866CB[2]	Evaluation Board			
EVAL-CONTROL BOARD[3]	Controller Board			

NOTES
[1]RU = TSSOP.
[2]This can be used as a stand-alone evaluation board or in conjunction with the EVAL-CONTROL BOARD for evaluation/demonstration purposes.
[3]This board is a complete unit allowing a PC to control and communicate with all Analog Devices evaluation boards ending in the CB designators.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7866 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	REF SELECT	Internal/External reference selection pin. Logic Input. If this pin is tied to GND then the on-chip 2.5V reference is used as the reference source for both ADC A and ADC B. In addition, pins V_{REF}, $D_{CAP}A$ and $D_{CAP}B$ must be tied to decoupling capacitors. If the REF SELECT pin is tied to a logic high, then an external reference can be supplied to the AD7866 through the V_{REF} pin, in which case decoupling capacitors are required on $D_{CAP}A$ and $D_{CAP}B$. However, if the V_{REF} pin is tied to AGND while REF SELECT is tied to a logic low, then an individual external reference can be applied to both ADC A and ADC B through pins $D_{CAP}A$ and $D_{CAP}B$ respectively.
2 9	$D_{CAP}B$ $D_{CAP}A$	Decoupling capacitors are connected to these pins to decouple the reference buffer for each respectiveADC. The internal reference can be taken from these pins and applied externally to the rest of a system. Depending on the polarity of the REF SELECT pin and the configuration of the V_{REF} pin, these pins can also be used to input a seperate external reference to each ADC. The range of the external reference input is dependant on the analog input range selected.
3,8	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7866. All analog input signals and any external reference signal should be referred to this AGND voltage. Both of these pins should connect to the AGND plane of a system. The AGND and DGND voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis.
4 5	V_{B2} V_{B1}	Analog Inputs of ADC B. Single-ended analog input channels. The input range on each channel is 0V to V_{REF} or 0V to $2*V_{REF}$ depending on the polarity of the RANGE pin.
6 7	V_{A2} V_{A1}	Analog Inputs of ADC A. Single-ended analog input channels. The input range on each channel is 0V to V_{REF} or 0V to $2*V_{REF}$ depending on the polarity of the RANGE pin.
10	V_{REF}	Reference Decoupling Pin and external reference selection pin. This pin is connected to the internal reference and requires a decoupling capacitor. The nominal reference voltage is 2.5V and this appears at the pin, however if the internal reference is to be used externally in a system then it must be taken from either the $D_{CAP}A$ or $D_{CAP}B$ pins. This pin is also used in conjunction with the REF SELECT pin when applying an external reference to the AD7866. See REF SELECT pin description.
11	RANGE	Analog input range and output coding selection pin. Logic Input. The polarity on this pin will determine what input range the analog input channels on the AD7866 will have and it will also select what type of output coding the ADC will use for the conversion result . On the falling edge of $\overline{CS}$ the polarity of this pin is checked to deter mine the analog input range of the next conversion. If this pin is tied to a logic low then the analog input range is 0V to V_{REF} and the output coding from the part will be straight binary (for the next conversion). If this pin is tied to a logic high when $\overline{CS}$ goes low, then the analog input range is 0V to $2*V_{REF}$ and the output coding for the part will be 2s complement. However, if after the falling edge of $\overline{CS}$, the logic level of the RANGE pin has changed upon the 8th SCLK edge then the output coding will change to the other option without any change in the analog input range. (See Analog Input and ADC Transfer Function sections.)
12	AV_{DD}	Analog Supply Voltage, +2.7V to +5.25V. This is the only supply voltage for all analog circuitry on the AD7866. The AV_{DD} and DV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to AGND.
13	DV_{DD}	Digital Supply Voltage, +2.7V to +5.25V. This is the supply voltage for all digital circuitry on the AD7866. The DV_{DD} and AV_{DD} voltages should ideally be at the same potential and must not be more than 0.3V apart even on a transient basis. This supply should be decoupled to DGND.
14	DGND	Digital Ground. This is the ground reference point for all digital circuitry on the AD7866. The DGND and AGND voltages should ideally be at the same potential and must not be more than 0.3V apart even on a tran sient basis.
15 16	$D_{OUT}A$, $D_{OUT}B$	Serial data outputs. The data output is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data appears on both pins simultaneously from the simultaneous conversions of both ADCs. On the AD7866, the data stream consists of one leading zero followed by three STATUS bits, followed by the 12 bits of conversion data. The data is provided MSB first. If $\overline{CS}$ is held low for a further 16 SCLK cycles after the conversion data has been output on either $D_{OUT}A$ or $D_{OUT}B$, then the data from the other ADC follows on the D_{OUT} pin. This allows data from a simultaneous conversion on both ADCs to be gathered in serial format on either $D_{OUT}A$ or $D_{OUT}B$ alone using only one serial port. See serial interface section.
17	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines what voltage the interface will operate at.
18	SCLK	Serial Clock. Logic Input. SCLK provides the SCLK for accessing the data from the AD7866. This clock is also used as the clock source for the conversion process.
19	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7866 and also frames the serial data transfer.
20	A0	Multiplexer select. Logic Input. This input is used to select which channel of each ADC is to be converted simulataneously, i.e. channel 1 of ADC A and channel 1 of ADC B, or channel 2 of ADC A and channel 2 of ADC B. If this pin is tied to a logic low then the conversion will be performed on channel 1 of each ADC, or if it is tied to a logic high then the conversion will be perfomed on channel 2 of each ADC.

TERMINOLOGY

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a point 1/2 LSB below the first code transition, and full scale, a point 1/2 LSB above the last code transition.

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Offset Error
This is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, i.e AGND + 1LSB

Offset Error Match
This is the difference in Offset Error between the two channels.

Gain Error
This is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal (i.e., V_{REF} – 1 LSB) after the offset error has been adjusted out.

Gain Error Match
This is the difference in Gain Error between the two channels.

Track/Hold Acquisition Time
The track/hold amplifier returns into track mode after the end of conversion. Track/Hold acquisition time is the time required for the output of the track/hold amplifier to reach its final value, within ±1/2 LSB, after the end of conversion.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the A/D converter. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process; the more levels, the smaller the quantization noise. The theoretical signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by:

Signal to (*Noise* + *Distortion*) = (6.02 *N* + 1.76) *dB*

Thus for a 12-bit converter, this is 74 dB and for a 10-bit converter is 62dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7866, it is defined as:

$$THD\ (dB) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$ and excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it will be a noise peak.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation distortion terms are those for which neither m nor n are equal to zero. For example, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

The AD7866 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second order terms are usually distanced in frequency from the original sine waves while the third order terms are usually at a frequency close to the input frequencies. As a result, the second and third order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in dBs.

PSR (Power Supply Rejection)
See Typical performance Curves section.

MODES OF OPERATION

The mode of operation of the AD7866 is selected by controlling the (logic) state of the $\overline{CS}$ signal during a conversion. There are three possible modes of operation, Normal Mode, Partial Power-Down Mode and Full Power-Down Mode. The point at which $\overline{CS}$ is pulled high after the conversion has been initiated will determine which power-down mode, if any, that the device will enter. Similarly, if already in a power-down mode then $\overline{CS}$ can control whether the device will return to Normal operation or remain in power-down. These modes of operation are designed to provide flexible power management options. These options can be chosen to optimize the power dissipation/throughput rate ratio for differing application requirements.

Normal Mode

This mode is intended for fastest throughput rate performance as the user does not have to worry about any power-up times with the AD7866 remaining fully powered all the time. Figure 2 shows the general diagram of the operation of the AD7866 in this mode.

The conversion is iniated on the falling edge of $\overline{CS}$ as described in the Serial Interface section. To ensure the part remains fully powered up at all times $\overline{CS}$ must remain low until at least 10 SCLK falling edges have elapsed after the falling edge of $\overline{CS}$. If $\overline{CS}$ is brought high any time after the 10th SCLK falling edge but before the 16th SCLK falling edge, the part will remain powered up but the conversion will be terminated and $D_{OUT}A$ and $D_{OUT}B$ will go back into tri-state. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The D_{OUT} line will not return to tri-state after 16 SCLK cycles have elapsed until CS is brought high again. If $\overline{CS}$ is left low for a further 16 SCLK cycles then the result from the other ADC on board will also be accessed on the same D_{OUT} line as shown in figure 8 (see serial Interface Section). The STATUS bits provided prior to each conversion result will identify which ADC the following result will be from. Once 32 SCLK cycles have elapsed then the D_{OUT} line will return to tri-state on the 32nd SCLK falling edge. If CS is brought high prior to this then the D_{OUT} line will return to tri-state at that point. Hence, $\overline{CS}$ may idle low after 32 SCLK cycles, until it is brought high again sometime prior to the next conversion, (effectively idling $\overline{CS}$ low), if so desired, as the bus will still return to tri-state upon cmpleteion of the read.

Once a data transfer is complete and $D_{OUT}A$ and $D_{OUT}B$ have returned to tri-state, another conversion can be initiated after the quiet time, t_{quiet}, has elapsed by bringing $\overline{CS}$ low again.

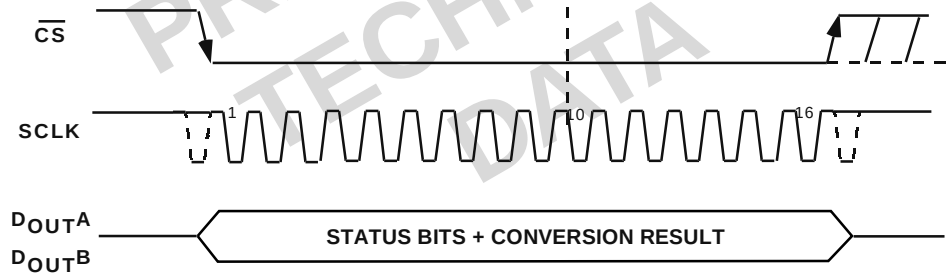


Figure 2. Normal Mode Operation

Partial Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required; either the ADC is powered down between each conversion, or a series of conversions may be performed at a high throughput rate and then the ADC is powered down for a relatively long duration between these bursts of several conversions. When the AD7866 is in partial power down, all analog circuitry is powered down except for the on-chip reference and reference buffer.

To enter Partial Power-Down, the conversion process must be interrupted by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK as shown in Figure 3. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will enter partial power down and the conversion that was intiated by the falling edge of $\overline{CS}$ will be terminated and $D_{OUT}A$ and $D_{OUT}B$ will go back into tri-state. If $\overline{CS}$ is brought high before the second SCLK falling edge, then

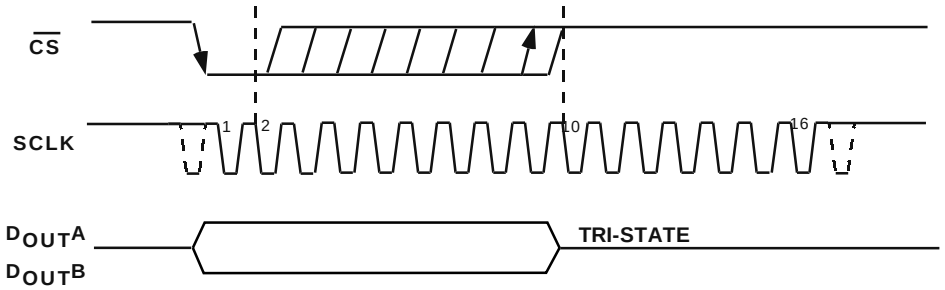


Figure 3. Entering Partial Power Down Mode

the part will remain in Normal Mode and will not power-down. This will avoid accidental powerdown due to glitches on the $\overline{CS}$ line.

In order to exit this mode of operation and power the AD7866 up again, a dummy conversion is performed. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The device will be fully powered up once 16 SCLKs have elapsed and valid data will result from the next conversion as shown in figure 4. If $\overline{CS}$ is brought high before the second falling edge of SCLK, then the AD7866 will go back into partial power down again. This avoids accidental power up due to glitches on the $\overline{CS}$ line, as although the device may begin to power up on the falling edge of $\overline{CS}$, it will power down again on the rising edge of $\overline{CS}$. If in Partial Power-Down and CS is brought high between the second and tenth falling edges of SCLK then the device will enter Full Power Down Mode.

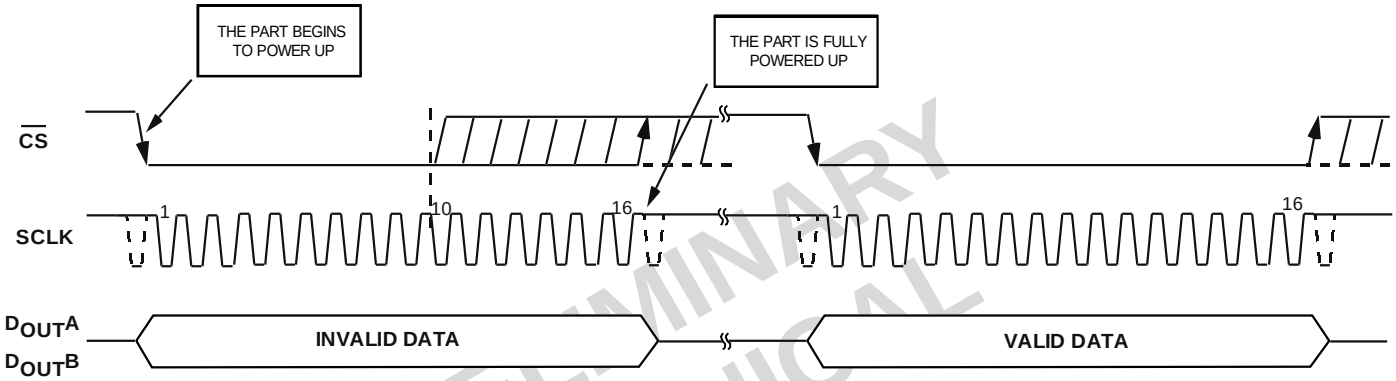


Figure 4. Exiting Partial Power-Down Mode

Full Power-Down Mode

This mode is intended for use in applications where slower throughput rates are required than that in the Partial Power Down Mode, as power up from a full power down would not be complete in just one dummy conversion. This mode is more suited to applications where a series of conversions performed at a relatively high throughput rate would be followed by a long period of inactivity and hence power down. When the AD7866 is in full power down, all analog circuitry is powered down. See Power-up Times section.

Full Power-Down is entered in a similar way as partial power down except the timing sequence shown in Figure 3 must be executed twice.The conversion process must be interrupted in a similar fashion by bringing $\overline{CS}$ high anywhere after the second falling edge of SCLK and before the tenth falling edge of SCLK. The device will enter partial power down at this point. To reach full power down, the next conversion cycle must be interrupted in the same way as shown in Figure 14. Once $\overline{CS}$ has been brought high in this window of SCLKs, then the part will power down completely.

NOTE: It is not necessary to complete the 16 SCLKs once $\overline{CS}$ has been brought high to enter a power down mode.

To exit Full Power Down, and power the AD7866 up again, a dummy conversion is performed as when power-

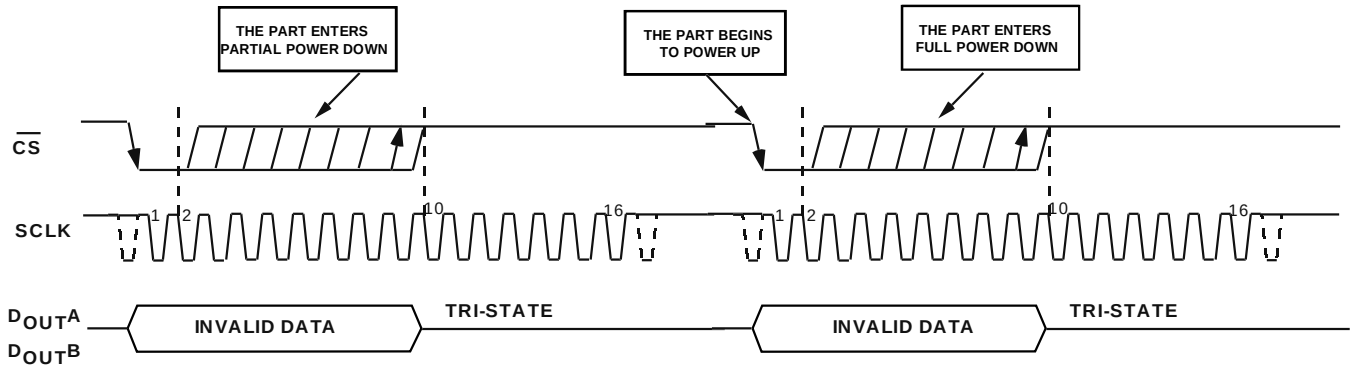


Figure 5. Entering Full Power-Down Mode

ing up from partial power down. On the falling edge of $\overline{CS}$ the device will begin to power up, and will continue to power up as long as $\overline{CS}$ is held low until after the falling edge of the tenth SCLK. The power up time is longer than one dummy conversion cycle however and this time must elapse before a conversion can be initaited as shown in Figure 6. See Power-up Times section for the power up times associated with the AD7866.

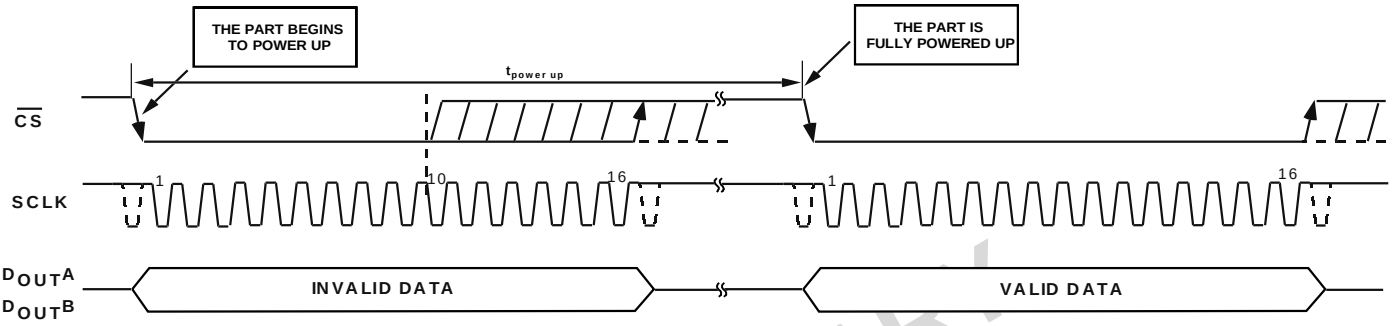


Figure 6. Exiting Full Power-Down Mode

SERIAL INTERFACE

Figure 7 shows the detailed timing diagram for serial interfacing to the AD7866. The serial clock provides the conversion clock and also controls the transfer of information from the AD7866 during conversion.

The $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ puts the track and hold into hold mode, takes the bus out of tristate and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete. Once 13 SCLK falling edges have elapsed, then the track and hold will go back into track on the next SCLK rising edge as shown in figure 7 at point B. On the rising edge of $\overline{CS}$, the conversion will be terminated and DoutA and DoutB will go back into tri-state. If CS is not brought high but instead held low for a further sixteen SCLK cycles on $D_{OUT}A$ then the data from conversion B will be output on $D_{OUT}A$. Likewise if CS is held low for a further sixteen SCLK cycles on $D_{OUT}B$ then the data from conversion A will be output on $D_{OUT}B$. This is illustrated in figure 8 where the case for $D_{OUT}A$ is shown. Sixteen serial clock cycles are required to perform the conversion process and to access data from one conversion on either data line of the AD7866. $\overline{CS}$ going low provides the leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges beginning with the first of three data STATUS bits , thus the first falling clock edge on the serial clock has the leading zero provided and also clocks out the first of three STATUS bits. The final bit in the data transfer is valid on the sixteenth falling edge, having being clocked out on the previous (15th) falling edge. In applications with a slower SCLK, it is possible to read in data on each SCLK rising edge, i.e. the first rising edge of SCLK after the $\overline{CS}$ falling edge would have the leading zero provided and the 15th rising SCLK edge would have DB0 provided.

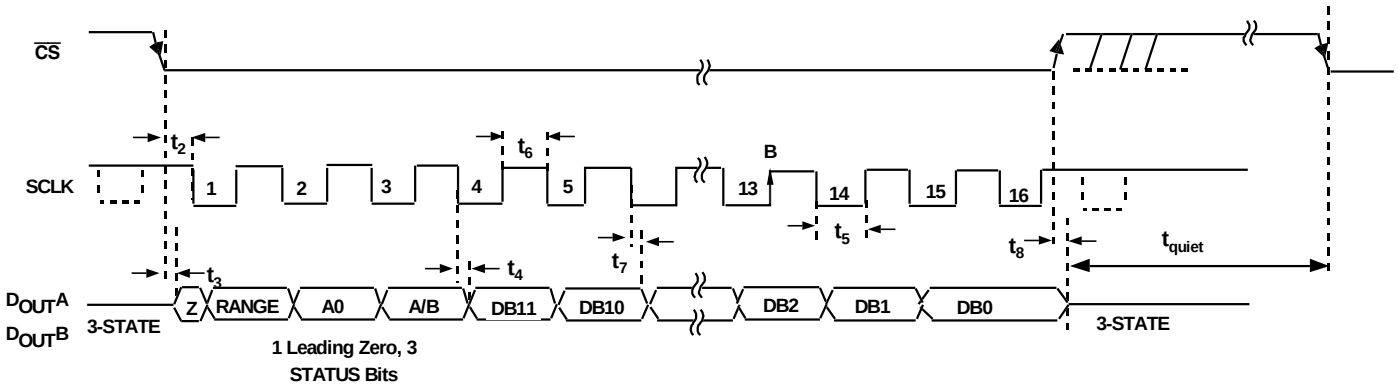


Figure 7. AD7866 Serial Interface Timing Diagram

The three STATUS bits which follow the leading zero provide information with respect to the conversion result which follows them on the D_{OUT} line in use. Table I shows how these identification bits can be interpreted.

STATUS BIT DESCRIPTION

Bit	Mnemonic	Comment
15	ZERO	Leading Zero. This bit will always be a zero output.
14	RANGE	The polarity of this bit reflects the analog input range that has been selected with the RANGE pin. If it is a 0 then it means in the previous transfer upon the falling edge of the CS the range pin was at a logic low providing an analog input range from 0V to V_{REF} for this conversion. If it is a 1 then it means in the previous transfer upon the falling edge of CS the RANGE pin was at a logic high resulting in an analog input range of 0V to $2*V_{REF}$ selected for this conversion. See Analog Input section.
13	A0	This bit indicates which channel the conversion is being performed on, channel 1 or channel 2 of the ADC in question. If this bit is a 0 then the conversion result will be from channel 1 of the ADC, and if it is a 1 then the result will be from channel 2 of the ADC in question.
12	A/B	This bit indicates which ADC the conversion result is from. If this bit is a 0 then the result is from ADC A, and if it is a 1 then the result if from ADC B. This is especially useful if only one serial port is available for use and one D_{OUT} line is used, as shown in figure 8.

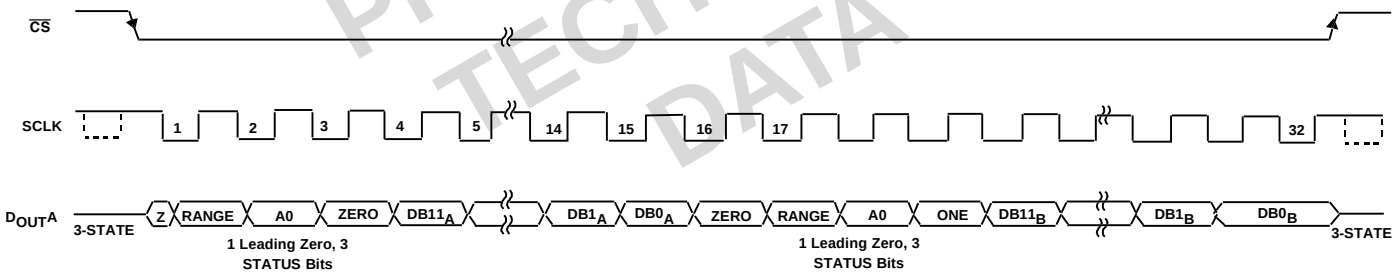


Figure 8. Reading data from both ADCs on one D_{OUT} line

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

20-Lead Tiny Shrink Small Outline Package (RU-20)